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Job Detail

Executive Level

Position Title	RTL Design and Verification Engineer
Recruiter Company	Fidel Consulting KK
Company Name	Company name is private
Activated / Updated	2024-05-10 / 2024-05-10
Job Type	IT (PC, Web, Unix) - Web Application SE IT (PC, Web, Unix) - Database SE IT (Mainframe) - Application SE
Industry	
Location	Asia Japan Tokyo
Job Description	Have the following experience in logic circuit design Able to describe detailed timing charts based on functional requirements. Formulate detailed specifications from functional requirements and create circuit block diagrams. Understanding clock synchronization and designing appropriate synchronization circuits Understand STARC rules and be able to code Experience on ARM CPU and/or its bus (AHB/AXI) Experience on Linux OS Define the pass/fail judgment method and its criteria from the verification items. Have the following experience in logic circuit verification Test pattern can be created and verified according to the contents of the verification item Define the values and precision that signals can take and define the bit width of each signal. Expand mathematical operations to define the optimal circuit configuration Understand FPGA/ASIC primitives and design RAM configurations and arithmetic circuits Have a basic understanding of Static Timing Analysis (STA)
Company Info	Over 300 customers, including 40% of the top 100 global innovators, to deliver intelligent engineering and technology solutions for creating a digital, autonomous, and sustainable future. As a company, is committed to designing a culturally inclusive, socially responsible, and environmentally sustainable Tomorrow Together with our stakeholders.
Qualifications	Technical Graduate with 4+ years of relevant experience Bilingual with good written and Verbal Communication JLPT/NAT certified
English Level	Business Conversation Level (TOEIC 735-860)
Japanese Level	Business Level(JLPT Level 2 or N2)
Salary	JPY - Japanese Yen JPY 3000K - JPY 7000K